W600 Specification

V1.0.2

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文档历史

Version	Date	Revision Record	Author	Approver	Auditor
V1.0.0	2018-03-29	Initial release	Ray	Tao	
V1.0.1	2019-02-20	Add 2MFlash discription	Ray		
V1.0.2	2019-4-20	Modify PWM pin number	Ray		

Content

1 Features

- Chip Packaging
  - Package QFN32, 5mm x 5mm
- Chip Integration
  - Integrated 32bit Embedded Cortex-M3 CPU, operating frequency 80MHz;
  - Integrated 288KB RAM;
  - Integrated 1MB/2MB FLASH;
  - Integrated 8 channel DMA controller. The hardware and software can use any free channel. DMA controller has 16 hardware requests, support software chain table;
  - Integrated 2.4G RF transceiver, support IEEE802.11 protocol;
  - Integrated PA/LNA/TR-Switch;
  - Integrated 32.768KHz oscillator;
  - Integrated voltage detection circuit;
  - Integrated LDO;
  - Integrated power supply control circuit;
  - Integrated power on reset circuit;
  - Integrated encrypted hardware accelerator, support PRNG, SHA1, MD5, RC4, DES, 3DES, AES, CRC;
- Chip Interface
  - Integrated one SDIO2.0 Device controller, support SDIO 1-/4-bit and SPI operating mode; operating frequency 0~50MHz;
  - Integrated 2 UART interface, support RTS/CTS, baud rate: 1200bps~2Mbps;
  - Integrated one high speed SPI controller, operating frequency: 0~50MHz;
  - Integrated one SPI master/slave mode, in master mode the data transmission rate is 20Mpbs, in slave mode the data transmission rate is 6Mbps;
  - Integrated one I²C controller, support data transmission rate 100/400Kbps;
  - Integrated GPIO controller;
  - Integrated PWM controller, support 5 channel PWM output or 2 channels PWM input capture. Max output frequency is 20MHz and max input frequency is 20MHz;
  - Integrated I²S controller, support full duplex and codec from 32KHz to 192KHz;
  - Integrated 7816 interface, support ISO-7816-3 T=0/1, EVM2000 protocol and UART protocol;
- Wi-Fi Protocol and function
  - Support GB15629.11-2006、IEEE802.11 b/g/n/e/i/d/k/r/s/w;
  - Support WAPI2.0;
  - Support Wi-Fi WMM/WMM-PS/WPA/WPA2/WPS;
  - Support Wi-Fi Direct;
  - Support EDCA channel access;
  - Support 20/40M bandwidth;
  - Support STBC, Greenfield, Short-GI and reverse transmission;
  - Support RIFS interframe space;
  - Support AMPDU, AMSDU;
  - Support IEEE802.11n MCS 0~7, MCS32, transmission rate is up to 150Mbps;
  - Support Short Preamble in 2/5.5/11Mbps;
  - Support HT-immediate Compressed Block Ack, Normal Ack, No Ack;

- Support CTS to self;
- Support AP function;
- Support used as AP and STA at the same time;
- Support up to 32 multicast networks with different encryption methods in BSS;
- As AP in BSS, the sum of sites and groups is up to 32 and in IBSS is up to 16;
- Reception sensitivity：
  - 20MHz MCS7@-71dBm;
  - 40MHz MCS7@-68dBm;
  - 54Mbps@-73dBm;
  - 11Mbps@-86dBm;
  - 1Mbps@-95dBm;
- Permissible carrier frequency deviation：50ppm;
- Permissible sampling frequency deviation：50ppm;
- Support STA with different encryption modes;
- Support multiple filtering options in reception frame;
- Support listen mode;

- Power Supply
  - 3.3V power supply;
  - Support PS-Poll, U-APSD low power management;
  - Standby power consumption less than 10uA;

2 General Description

W600 is an embedded Wi-Fi SoC chip which is complying with IEEE802.11b/g/n (1T1R) international standard and which supports multi interface, multi-protocol. It can be easily applied to smart appliances, smart home, health care, smart toy, and wireless audio & video, industrial and other IoT fields.

3 Overview

This SoC integrates Cortex-M3 CPU, Flash, RF Transceiver, CMOS PA, Baseband control. It applies multi interfaces such as SDIO, SPI, UART, GPIO, I²C, PWM, I²S, 7816 etc. It applies multi encryption and decryption protocol such as PRNG, SHA1, MD5, RC4, DES, 3DES, AES, CRC etc.

4 Block Diagram

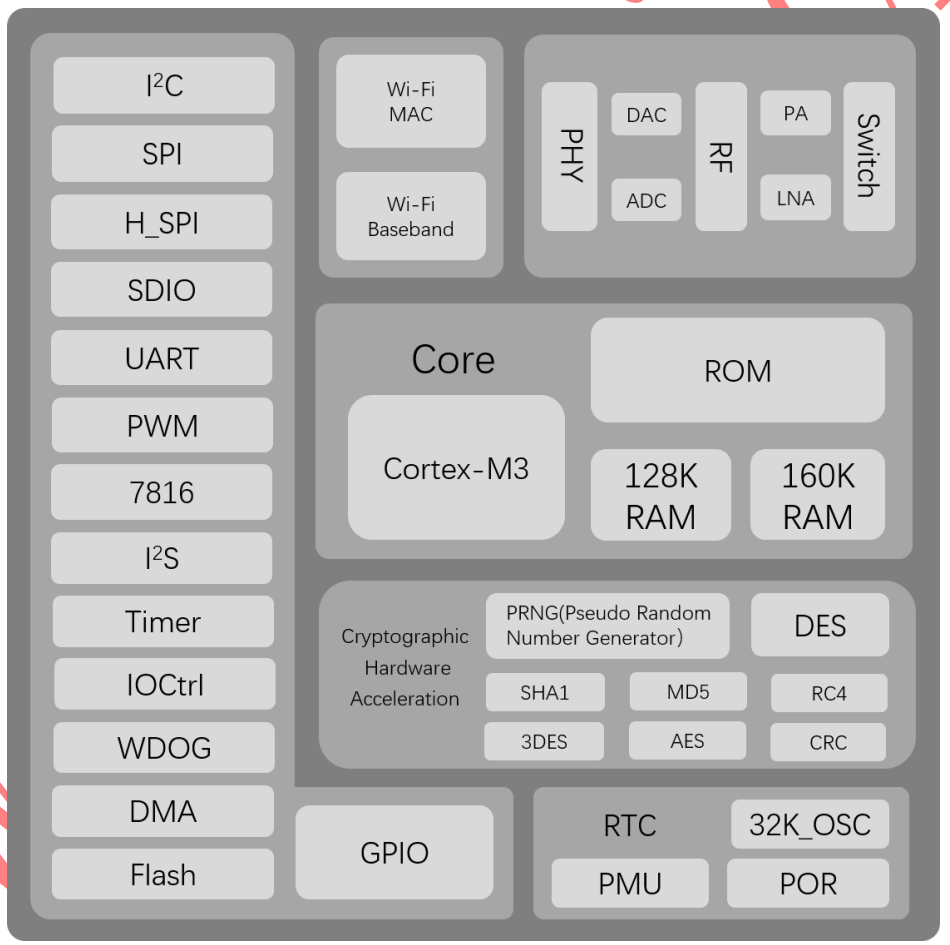

Figure 4-1 W600 Block Diagram

5 System Memory Map

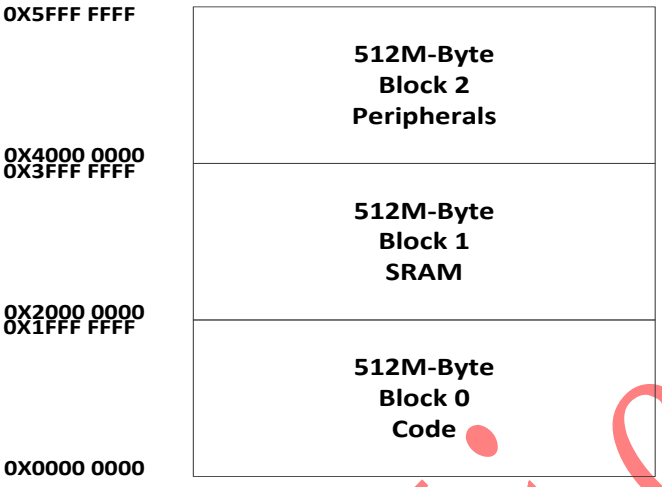

Figure 5-1 Address Space Assignments

Table 5-1 Peripheral Address Space Assignments

Peripheral	BootMode=0	BootMode=1	Address Space	Description
ROM	0x00000000 ~ 0x0003FFFF	0x1FF00000 ~ 0x1FF3FFFF		Firmware
FLASH	0x08000000 ~ 0x081FFFFF	0x00000000 ~ 0x001FFFFF		Specific instruction Memory Space
SRAM	0x20000000 ~ 0x20027FFF	0x20000000 ~ 0x20027FFF		Firmware and instruction memory space
MAC RAM	0x20028000 ~ 0x2003FFFF	0x20028000 ~ 0x2003FFFF		SDIO/H_SPI/UART data buffer
CONFIG	0x40000000 ~ 0x40001FFF	0x40000000 ~ 0x40001FFF	0x40000000 ~ 0x400001FF	SDIO
			0x40000200 ~ 0x400002FF	SPI
			0x40000300 ~ 0x400003FF	SDIO Wrapper
			0x40000400 ~ 0x400005FF	DMA
			0x40000600 ~ 0x400006FF	PMU
			0x40000700 ~ 0x400007FF	Clock and Reset
			0x40000800 ~ 0x400009FF	
			0x40000A00 ~ 0x400013FF	
			0x40001400 ~ 0x400017FF	

			0x40001800 ~ 0x40001FFF	
			0x40002000 ~ 0x400021FF	FLASH Controller
			0x40002200 ~ 0x400028FF	RSA
			0x40003200 ~ 0x400033FF	GPSEC
APB	0x40010000 ~ 0x4003C000	0x40010000 ~ 0x4003C000	0x40010000 ~ 0x400101FF	I^2C Master
			0x40010200 ~ 0x400103FF	
			0x40010400 ~ 0x400107FF	SPI Master
			0x40010800 ~ 0x400109FF	UART0
			0x40010A00 ~ 0x40010BFF	UART1
			0x40010C00 ~ 0x40010DFF	GPIOA
			0x40010E00 ~ 0x40010FFF	Timer
			0x40011000 ~ 0x400111FF	WDOG
			0x40011200 ~ 0x400113FF	GPIOB
			0x40011400 ~ 0x400115FF	
			0x40011600 ~ 0x400117FF	
			0x40011800 ~ 0x400119FF	PWM
			0x40011A00 ~ 0x40011BFF	I^2S
			0x40011C00 ~ 0x40011DFF	7816/UART2
			0x40014000 ~ 0x4000BFFF	
			0x4001C000 ~ 0x4003BFFF	
			0x40013C00 ~ 0x5FFFFFFF	RSV

6 Functional Description

6.1 SDIO Controller

SDIO Controller transfer data with host and it has 1024 Bytes FIFO.

- Support SDIO2.0;

- Support frequency from 0 to 50MHz;
- Support block size up to 1024 bytes;
- Support soft reset;
- Support SPI, 1bit SD mode and 4 bits SD mode;

6.2 High speed SPI Controller

Support SPI protocol, has configurable data frame. The maximum data rate is 50Mbp.

- Support SPI protocol;
- Support alternative interrupt signal;
- Support max data rate 50Mbps;
- hardware decode and DMA data transfer;

6.3 DMA Controller

Support 8 channel, 16 DMA request signals, has chain table and register configuration.

- Support Amba2.0 protocol, 8 DMA channel;
- Support chain table operating mode;
- 16 configurable DMA request signals;
- Support 1,4-burst data transfer;
- Support byte-, half-word-, word- access;
- Programmable source or destination address unchanged, sequentially increases or pre-defined;
- Synchronous DMA request and DMA response timing;

6.4 Clock and Reset Controller

Support the control of clock and reset system. Clock control includes clock frequency conversion, clock turn off and adaptive gating, and reset control includes soft reset control of system and sub modules.

6.5 Memory Controller

Support the cache size configuration during transmitting and receiving, MAC access base address, cache number and frame aggregation control signals.

6.6 BBP

Support IEEE802.11a/b/g/e/n (1T1R). The main features are:

- Data rate: 1~54Mpbs (802.11a/b/g), 6.5~150Mbps (802.11n);
- MCS data format： MCS0~MCS7,MCS32(40MHz HT Duplicate mode);
- Support 40MHz bandwidth non-HT Duplicate mode, 6M～54M;

- Signal bandwidth：20MHz, 40MHz;
- Modulation mode：DSSS(DBPSK,DQPSK,CCK) and OFDM(BPSK,QPSK,16QAM,64QAM);
- Support 1T1R MIMO-OFDM spatial multiplexing;
- Support Short GI mode;
- Support legacy mode and Mixed mode;
- Support data transmission and reception on 20M upper and low side in 40MHz bandwidth;
- Support STBC receive with MCS0～7, 32;
- Support Green Field;

6.7 MAC

Support IEEE802.11a/b/g/e/n MAC protocol. The main features of MAC are:

- Support EDCA channel access;
- Support CSMA/CA, NAV and TXOP;
- Support Beacon, Mng, VO, VI, BE, BK and QoS;
- Support unicast, broadcast and multicast;
- Support RTS/CTS,CTS2SELF,Normal ACK,No ACK frame format;
- Support retry and control of power and transmission rate;
- Support MPDU and Immediate BlockAck;
- Support RIFS,SIFS,AIFS;
- Support reverse transmission;
- Support programmable TSF Timer;
- Support MIB statistical information;

6.8 SEC

Support the security algorithm in IEEE802.11a/b/g/e/n protocol. Encryption or decryption in the process of transmitting and receiving data frames.

- Support throughput greater than 150Mbps;
- Support Amba2.0 bus protocol;
- Support WAPI2.0;
- Support WEP-64;
- Support WEP-128;
- Support TKIP;
- Support CCMP;

6.9 FLASH Controller

- Provide bus access in Flash interface;
- Provide arbitration between system bus and data bus;
- Implementation of CACHE;
- Support compatible with different QFlash;

6.10 RSA Encryption

RSA, arithmetic hardware coprocessor, provides Montgomery (FIOS) modular multiplication. The module implements of RSA algorithm with RSA software library, and supports from 128-bit to 2048-bit.

6.11 Encrypted Hardware Accelerator

The specified length data in the source address will be automatically en-/decrypted, and the result data will be write to the designated destination address space.

The module support PRNG (Pseudo random Number Generator), SHA1, MD5, RC4, DES, 3DES, AES, CRC.

6.12 I²C Controller

I²C Controller connects though APB Interface. Its supports master mode and configurable operating frequency（100K-400K）.

6.13 Master/Slave SPI Controller

Its support Master/Slave operating mode. The operating frequency is the frequency of system Bus. The main features of the bus are：

- Provides separate 8-level depth transmit and receive FIFO buffers;
- support Motorola SPI protocol,（CPOL,CPHA）, TI protocol, macrowire protocol in master mode;
- support Motorola SPI protocol（CPOL,CPHA）in slave mode;
- Support full duplex and half duplex;
- support data length up to 65535bit in master mode;
- support data transfer of any bit length in slave mode;
- 1/6 system clock frequency is max frequency of spi_clk in slave mode;

6.14 UART Controller

- Support APB bus protocol;
- Support Interrupt or polling;
- Support DMA, Separate receive/transmit 32 bytes entry FIFO buffer;
- Programmable baud rate;
- Programmable number of data bit, 5-8bit, and parity bit;
- Programmable stop bit, 1 or 2;
- Support auto flow control/flow control function;
- Support Break frame;
- Support interrupt of overrun, parity error, frame error, rx break frame;
- Up to 16-burst byte DMA data transfer;

6.15 GPIO Controller

Has 48-bit configurable GPIO, programmable input or output, configurable interrupt.
GPIOA and GPIOB have the same function with different base address.

6.16 Timer Controller

Configurable us or ms Timer, has 6 programmable 32-bit timers, Use interrupt flag to detect Time out.

6.17 Watchdog

The Watchdog is used to perform a system reset when system runs into an unknown state. The system software must respond to a periodic interruption, otherwise a hard reset will be generated.

6.18 RF Configurator

Support SPI bus protocol. The operating clock is system clock. The main features of the bus is：

- Provides separate 1-word depth transmit and receive FIFO buffers;

6.19 RF Transceiver

- The RF transceiver includes a power amplifier, a transmission channel, a receiving channel, a phase locked loop and a SPI, which changes the working state of the chip by the signals SHDN, RXEN and TXEN;
- The receiving channel uses the zero intermediate frequency structure to convert the RF signal directly

to the baseband I and Q output. The RF front end works in 2.4GHz, including low noise amplifier and orthogonal mixer. The baseband is composed of low pass filter and variable gain amplifier to realize channel filtering and gain control. The drive amplifier provides different DC output for the ADC interface.

- The transmission channel includes programmable control filter, upconverter mixer, variable gain amplifier and power amplifier. The transmission channel uses the output signal of direct frequency conversion structure. DAC signal through low pass filter, filter out the mirror frequency and out of band noise. PA output signal is differential output to drive antenna.

6.20 PWM Controller

- Has 5 PWM generators;
- Support 2 channels input capture (PWM0 and PWM4);
- Frequency range: 3Hz~160KHz;;
- Duty ratio precision: 1/256, Dead-Zone counter: 8bit;

6.21 I²S Controller

- Support AMBA APB bus protocol, 32bit single read/write;
- Operates as either Master or Slave, support full duplex;
- Capable of handling 8, 16, 24, 32 bits word size, sampling frequency is up to 128KHz;
- Support Mono and stereo audio data;
- Support I²S and MSB justified data format, support PCM A/B data format;
- Support DMA data transfer, word access only.

6.22 7816/UART Controller

- Support APB bus protocol;
- Support Interrupt or polling;
- Support DMA, Separate receive/transmit 32 bytes entry FIFO buffer;
- Support DMA data transfer, word access only. Up to 16-burst byte DMA data transfer;

Support UART and 7816 features：

UART features：

- Programmable baud rate;
- Programmable number of data bit, 5-8bit, and parity bit;
- Programmable stop bit, 1 or 2;
- Support auto flow control/flow control function (RTS/CTS);
- Support Break frame;
- Support interrupt of overrun, parity error, frame error, rx break frame;

7816 features:

- Support ISO-7816-3 T=0,T=1;
- Support EVM2000 protocol;
- Support guard time (11 ETU-267 ETU);
- Programmable inverse convention or direct convention;
- Support receive/transmit data frame with parity bit and retrans;
- Programmable stop bit, 0.5 or 1.5;

7 Pin Description

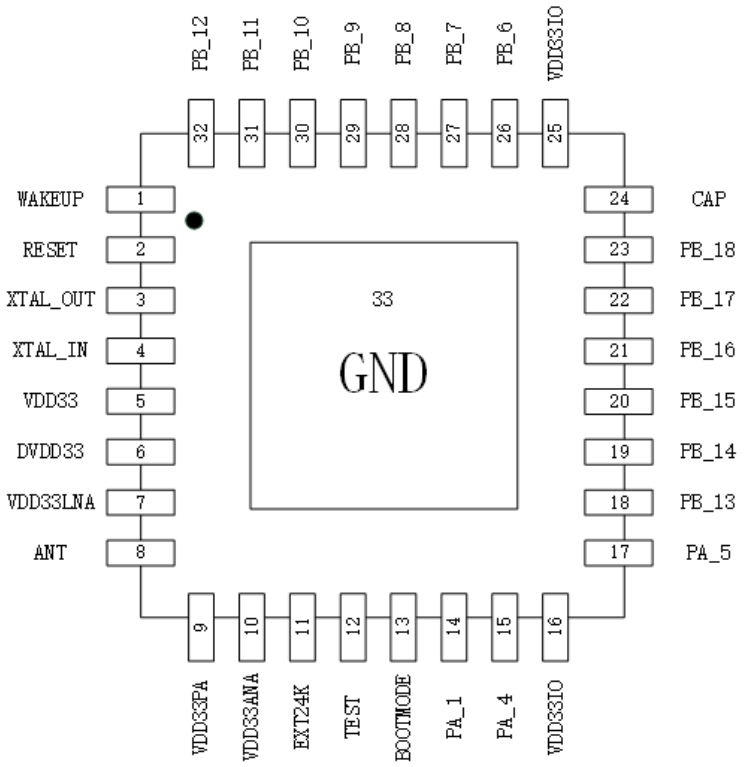

Figure 7-1 QFN32 pin Diagram

Table 7-1 Pin Description (QFN32)

Pin No.	Pin Name	Type	Function Description after reset	Multi-function
1	WAKEUP	I	WAKEUP	
2	RESET	I	RESET	
3	XTAL_OUT	O	Output External crystal oscillator	
4	XTAL_IN	I	input External crystal oscillator	
5	VDD33	P	power supply, 3.3V	
6	DVDD33	P	power supply for digital circuit, 3.3V	
7	VDD33LNA	P	power supply for LNA, 3.3V	
8	ANT	I/O	RF antenna	
9	VDD33PA	P	PA power supply, 3.3V	
10	VDD33ANA	P	power supply for analog circuit, 3.3V	
11	EXT24K	I	series connect with a resistor (24KΩ+-1%)	
12	TEST	I	Test mode	

13	BOOTMODE	I/O	BOOTMODE	PWM_0、GPIOPA_0
14	PA_1	I/O	Reserved	SIM_DATA、PWM_1、SPI(M/S)_CK、GPIOPA_1
15	PA_4	I/O	UART0_TX	PWM_4、SPI(M/S)_DO、I²S_M_SCL、GPIOPA_4
16	VDD33IO	P	IO power supply,3.3V	
17	PA_5	I/O	UART0_RX	PWM_0、SPI(M/S)_DI、I²S_M_EXTCLK、GPIOPA_5
18	PB_13	I/O	PWM_1	I²C_SCL、SDIO_CMD、GPIOPB_13
19	PB_14	I/O	H_SPI_INT	PWM_4、I²C_DAT、I²S_S_SDA、GPIOPB_14
20	PB_15	I/O	H_SPI_CS	PWM_3、SPI(M/S)_CS、I²S_S_SCL、GPIOPB_15
21	PB_16	I/O	H_SPI_CK	PWM_2、SPI(M/S)_CK、I²S_S_RL、GPIOPB_16
22	PB_17	I/O	H_SPI_DI	PWM_1、SPI(M/S)_DI、UART1_RX、GPIOPB_17
23	PB_18	I/O	H_SPI_DO	PWM_0、SPI(M/S)_DO、UART1_TX、GPIOPB_18
24	CAP	I	Capacitance,1μF	
25	VDD33IO	P	IO power supply, 3.3V	
26	PB_6	I/O	Reserved	SWDAT、UART0_RX、PWM_3、SIM_CLK、GPIOPB_6
27	PB_7	I/O	Reserved	SWCK、UART0_TX、SDIO_CMD、SPI(M/S)_CS、GPIOPB_7
28	PB_8	I/O	PWM_4	H_SPI_CK、SDIO_CK、I²S_M_SCL、GPIOPB_8
29	PB_9	I/O	UART1_CTS	H_SPI_INT、SDIO_DAT0、I²S_M_SDA、GPIOPB_9
30	PB_10	I/O	UART1_RTS	H_SPI_CS、SDIO_DAT1、I²S_M_RL、GPIOPB_10
31	PB_11	I/O	UART1_RX	H_SPI_DI、SDIO_DAT2、I²C_SCL、GPIOPB_11
32	PB_12	I/O	UART1_TX	H_SPI_DO、SDIO_DAT3、I²C_DAT、GPIOPB_12
33	GND	P	Ground	

1. I = Input, O = Output, P = Power Supply

8 Parameters

8.1 Ultimate Characteristics

Table 8-1 ultimate characteristic

Parameter	Symbol	Min	Typ	Max	Unit
VDD supply voltage	VDD	3.0	3.3	3.6	V
Input low voltage	V_{IL}	-0.3		0.8	V
Input high voltage	V_{IH}	2.0		VDD+0.3	V
Input capacitance	C_{pad}			2	pF
output low voltage	V_{OL}			0.4	V
output high voltage	V_{OH}	2.4			V
Max. output current	I_{MAX}			24	mA
Storage temperature	T_{STR}	-40℃		+125℃	℃
Operating temperature	T_{OPR}	-40℃		+85℃	℃

8.2 RF power parameters

Table 8-2 RF power parameters

Operation Mode	Typ	Unit
transmit IEEE802.11b, CCK 11Mbps, POUT = +19 dBm	230	mA
transmit IEEE802.11g, OFDM 54Mbps, POUT = +13.5 dBm	210	mA
transmit IEEE802.11n, OFDM MCS7, POUT = +12dBm	210	mA
receive IEEE802.11b/g/n	100-110	mA

8.3 Wi-Fi RF

Wi-Fi RF parameters

Parameter	Typ	Unit
Input frequency	2.4GHz~2.4835MHz	
Output Power		
72.2 Mbps PA Output Power	12	dBm
11b mode PA Output Power	19	dBm
Sensitivity		
DSSS, 1 Mbps	-95	dBm
CCK, 11 Mbps	-86	dBm
OFDM, 6 Mbps	-89	dBm

OFDM, 54 Mbps	-73	dBm
HT20, MCS0	-89	dBm
HT20, MCS7	-71	dBm
HT40, MCS0	-85	dBm
HT40, MCS7	-68	dBm
Adjacent Channel restrain		
OFDM, 6 Mbps	32	dB
OFDM, 54 Mbps	15	dB
HT20, MCS0	29	dB
HT20, MCS7	10	dB

9 Package Mechanical

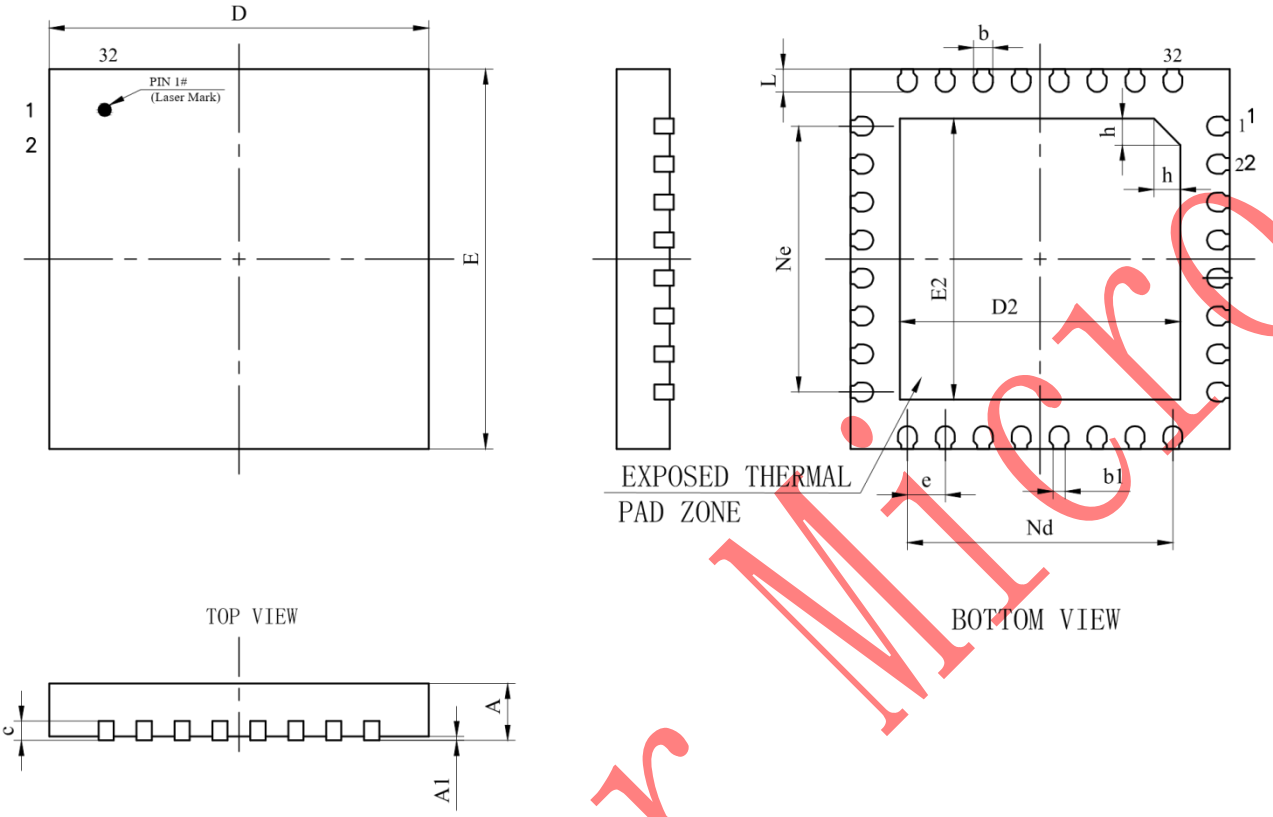

Figure 9-1 W600 package outline

Table 9-1 W600 package mechanical data

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.20	0.25	0.30
b1		0.16REF	
c	0.18	0.20	0.25
D	4.90	5.00	5.10
D2	3.70	3.80	3.90
e		0.50BSC	
Ne		3.50BSC	
Nd		3.50BSC	
E	4.90	5.00	5.10
E2	3.70	3.80	3.90

L	0.25	0.30	0.35
h	0.30	0.35	0.40
L/F carrier size	4.10x4.10		

10 Parts Information List

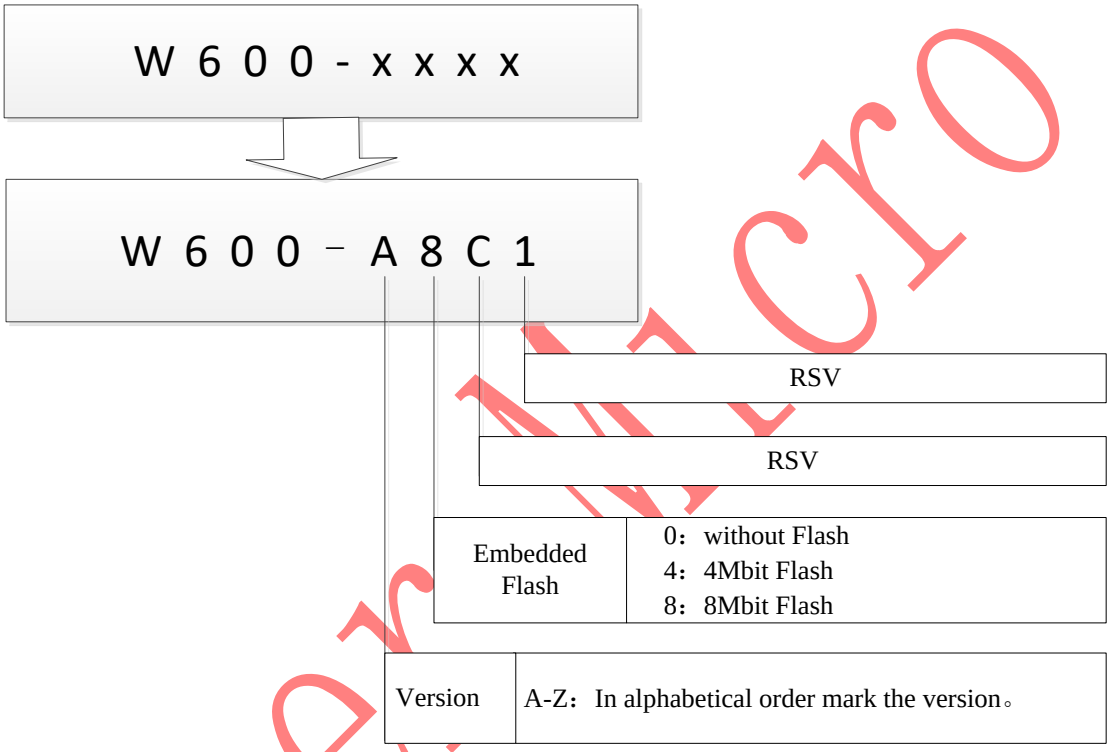

Figure 10-1 Ordering information scheme

For example:

- Integrate 1MByte Flash Type: W600-A800
- Integrate 2MByte Flash Type: W600-BA00