Comparison Sheet

Between W5100S and W5100

Version 1.1.0

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W5100S vs W5100

W5100S 는 W5100 를 기반으로 개발되었으나, W5100 과의 Hardware PIN-to-PIN Compatibility 를 지원하지 않고 Firmware Compatibility 만을 지원한다.

W5100S 는 W5100 과의 Firmware Compatibility 를 위해 W5100 Register Map 과 동일하게 구성되고, 기능 개선을 위해 Register 가 개선되거나 추가된다.

개선된 기능에 관해서는 W5100S Datasheet 를 참고 바란다.

W5100 은 PPPoE 연결 Process 들이 Fully Hardwired Logic 으로 구현된 반면, W5100S 는 다양한 PPPoE 연결 Option 처리를 위해, PPP LCP echo Replay 를 제외한 PPPoE 연결 Process 들은 Software 로 처리한다.

W5100S 는 그 외 ARP-Request, PING-Request 와 같은 SOCKET-less command 를 지원하고, Ethernet PHY register Access 를 지원하고, Power Save 를 위해 Ethernet PHY Power Down Mode 와 System Clock Switch 을 지원한다.

1 HOST Interface

	HOST Interface	W5100S	W5100
SPI	SCLK Period(1)	20ns	70ns
	MISO value on Write Data Phase(2)	0x00	0x03
Parallel Bus	ADDR	ADDR[1:0]	ADDR[14:0]
	Direct	X	O
	Indirect	O	O

Notice

(1) Refer to SPI Timing in each datasheet.

(2) SPI Frame

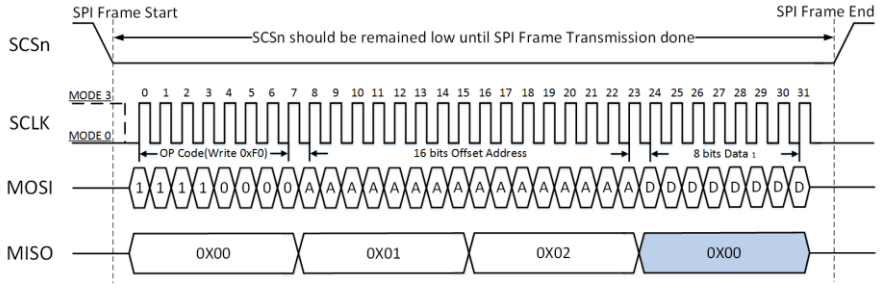

Figure 1 W5100S SPI Frame

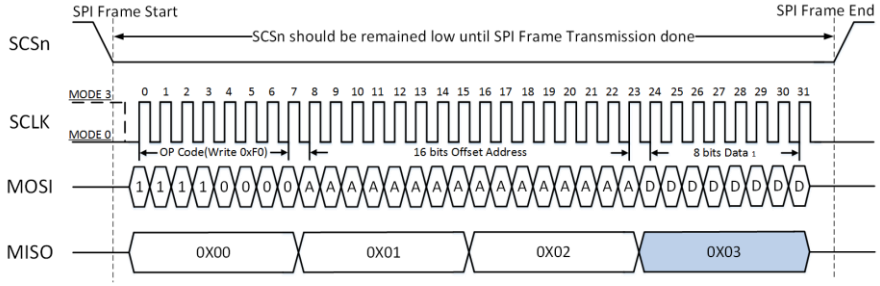

Figure 2 W5100 SPI Frame

2 Ethernet PHY Interface

Function	W5100S	W5100
Link LED	LNKn, No Blink (Hold Low)	LINKLED, Blink
RX/TX LED	-	RXLED, TXLED
Activity LED	ACTn	-
PHY Operation Mode	By Register PHYCR0[2:0]	By Pins OPMODE[2:0]
Ethernet PHY's Register	Accessible with PHYAR, PHYRR, PHYDIR, PHYDOR and PHYACR.	Inaccessible

3 Register

3.1 Change & Expansion

REG	W5100S	W5100
MR	AI : Always '1' IND : Always '1'	AI : Configurable IND : Configurable
Sn_MR	Removed PPPoE Mode	
Sn_SR	Removed the PPPoE SOCKET Status - SOCK_PPPOE, SOCK_CLOSING, SOCK_ARP	-
S0_CR	Removed the PPPoE Commands - PCON, PDISCON, PCR, PCN, PCJ	-
S0_IR	Removed the PPPoE Interrupts - PRECV, PFAIL, PNEXT	
Sn_TX_RR	Renamed Sn_TX_RD	-
Sn_RX_WR	Usable	Reserved
PHAR	Additional Dedicated Register for PPPoE Server Hardware Address	Shared with S0_DHAR
PSIDR	Additional Dedicated Register for PPPoE Session ID Register	Shared with S0_DPORT

3.2 Addition

REG	Description	Remark
INTPTMR	Interrupt Pending Time Register	Interrupt
IR2	Interrupt Register 2, For Wake On LAN(WOL) over UDP	
IMR2	Interrupt Register 2 Mask, For Mask IR2[WOL]	

MR2	Mode Register 2 cf> System clock can be selectable at 100MHz or 10MHz by MR2[CLKSEL]	Mode
PMRUR	Maximum Receive Unit Register on PPPoE	PPPoE
PHAR	PPPoE Server Hardware Address	
PSIDR	PPPoE Session ID	
PHYSR	PHY Status Register	Ethernet PHY
PHYAR	PHY Address Value Register (‘01010’)	
PHYRR	PHY Register Address Register	
PHYDIR	PHY Data Input Register	
PHYDOR	PHY Data Output Register	
PHYACR	PHY Action Register	
PHYDIVR	PHY Division Register	
PHYCR	PHY Control Register	
SLCR	SOCKET-less Command Register	SOCKET-less
SLRTR	SOCKET-less Retransmission Time Register	
SLRCR	SOCKET-less Retransmission Count Register	
SLPIPR	SOCKET-less Peer IP Address Register	
SLPHAR	SOCKET-less Peer Hardware Address Register	
PINGSEQR	PING Sequence-number Register	
PINGIDR	PING ID Register	
SLIMR	SOCKET-less Interrupt Mask Register	
SLIR	SOCKET-less Interrupt Register	
CLKLCKR	Clock Lock Register	Lock
NETLCKR	Network Lock Register	
PHYLCKR	PHY Lock Register	
VERR	Chip Version Register	Version
TCNTR	Ticker Count Register	Ticker
TCNTCLR	TCNTR Clear Register	
Sn_RXBUF_SIZE	SOCKET n Receive Buffer Size Register cf) W5100 과 같이 RMSR 을 통해서도 설정 가능하다.	SOCKET
Sn_TXBUF_SIZE	SOCKET n Transmit Buffer Size Register cf) W5100 과 같이 TMSR 을 통해서도 설정 가능하다.	
Sn_IMR	SOCKET n Interrupt Mask Register	
Sn_FRAGR	SOCKET n Fragment Offset in IP Header	
Sn_MR2	SOCKET n Mode Register 2	
Sn_KPALVTR	SOCKET n Keep-alive Timer Register	

Sn_RTR	SOCKET n Retransmission Time Register
Sn_RCR	SOCKET n Retry Count Register

3.3 Removal

REG	Description
PATR	Because some PPPoE Hardwired Logic is replaced with Software

4 Package

	W5100S	W5100
Package	W5100S-L 48 LQFP W5100S-Q 48 QFN	80 LQFP

5 Document Revision History

Version	Date	Descriptions
Ver. 1.0.0	1APR2018	Initial Release
Ver. 1.1.0	6ARP2018	1. Changed PHYRR to PHYRAR (in *3.2 Addition*) 2. Changed Retry to Retransmission in SLRCR (in *3.2 Addition*)