<VSECTOL OPTION>

Numerical convergence in Spice simulators is closely coupled to the concept of the error in numerical integration. Reducing the time step reduces numerical integration errors. The error boundary for the numerical integration is estimated and is the basis for setting the transient step time. For many circuits, simulations contain sharp voltage steps that are not constrained by numerical integration. When this occurs, integration accuracy is unaffected so that the simulator is allowed a large time step. This results in a loss in accuracy because the excessively large time steps can jump over needed details. In the past, it was necessary to restrict this behavior by setting Tmax in the .TRAN statement. The January 2000 newsletter (http://www.intusoft.com/nl59.htm) addressed this problem using the available simulation techniques. The problems arising out of the circuit used for the January 2000 newsletter caused us, here at Intusoft, to explore IsSpice code changes that can solve the problem in a more efficient manner. It turns out there was a code fragment left over from an earlier attempt by us to solve the problem, but was not implemented because we tried to reduce the time step until a specified voltage accuracy was achieved; an impossible task for a switching waveform.

Modifying the constraint, on the other hand, to test for a volt-second error produces the desired result. The latter method will always find a time step that is small enough while the earlier method will have a constant error as the time step is reduced.

We introduced a new option, VSECTOL, which reduces the time step if the product of the absolute value of the error in predicted voltage (prediction – solution) and the time step exceeds the VSECTOL specification. As in most IsSpice options, its default is zero, which turns the option off. In testing the new VSECTOL option, we ran some cases setting RELTO=0.5 and at the same time set VSECTOL to a reasonable value for the circuit. Figure 5 shows this new time step control option. Figures 6 and 7 show the results for a simplified power supply model versus the standard OPTIONS to control the time step. This introduces a completely new time step control for the simulation, based on node voltage accuracy. Using snubber.dwg, shown in Figure 5, as a test circuit we ran the usual analysis. All we needed to do was set VSECTOL=50n, RELTOL=.5 and BYPASS = OFF; no TMAX was needed in the .tran statement. On the other hand, many parameters were modified to get spice to run this circuit to completion, including setting TMAX to 20n. The VSECTOL controlled simulation ran faster and produced more detail in the switching transitions. The conventional simulation spent a lot of extra time when the circuit wasn't switching and took fewer points in the switching transition. The Bypass option controls whether or not the device operating point is calculated for each time step. When Bypass is ON, these load operations are skipped if errors are low enough. Since RELTOL is used in the calculations, we can't use the BYPASS

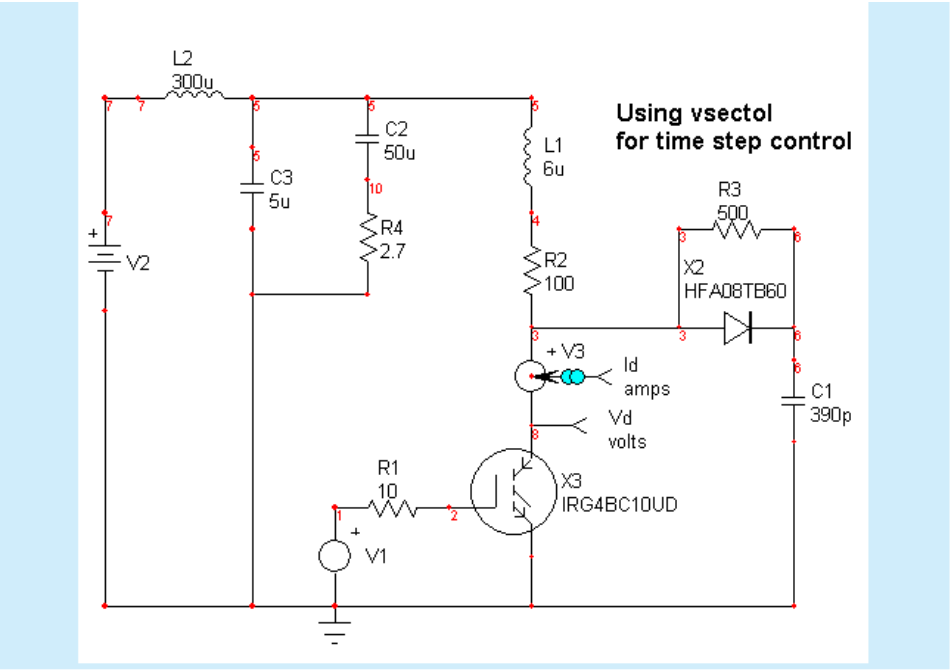

Figure 5. Snubber.dwg uses VSECTOL for time step control.

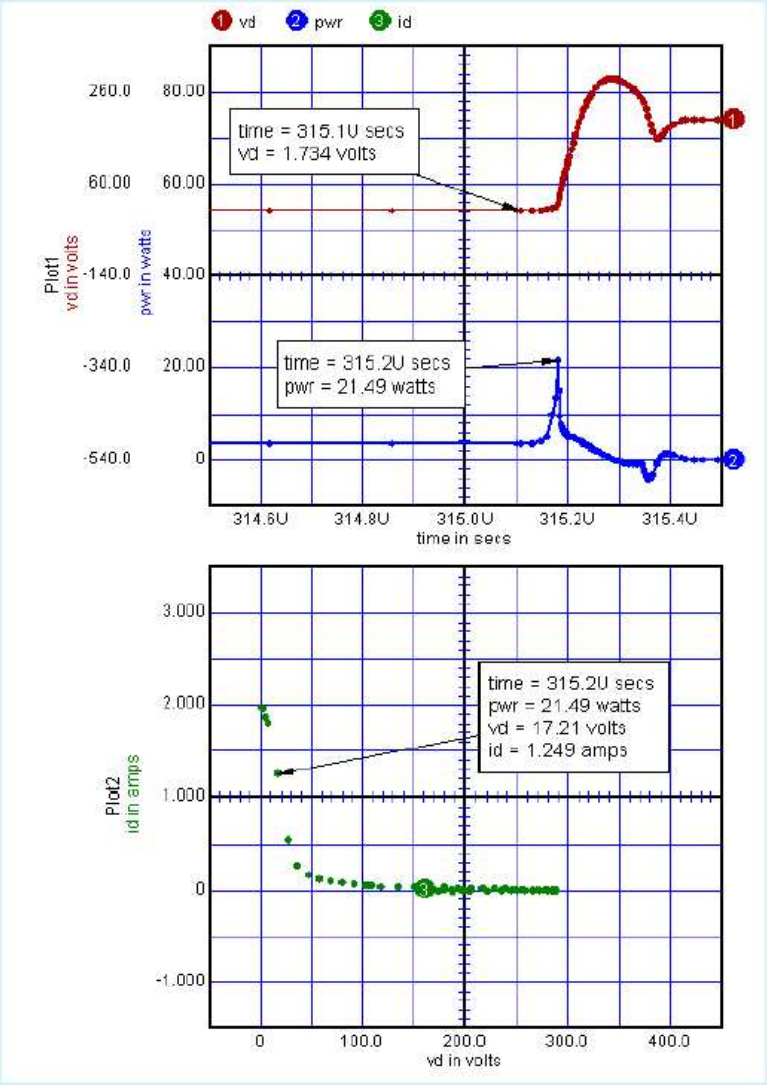

Figure 6. A simplified power supply model for switching transistor stress test and snubber design.

Result using VSECTOL to control the time step produces higher accuracy during the turn-off transition and uses less computational resources when there is no switching activity.

Transient timepoints = 26015
Accepted timepoints = 14217
Rejected timepoints = 11798
Total Analysis Time = 35.15

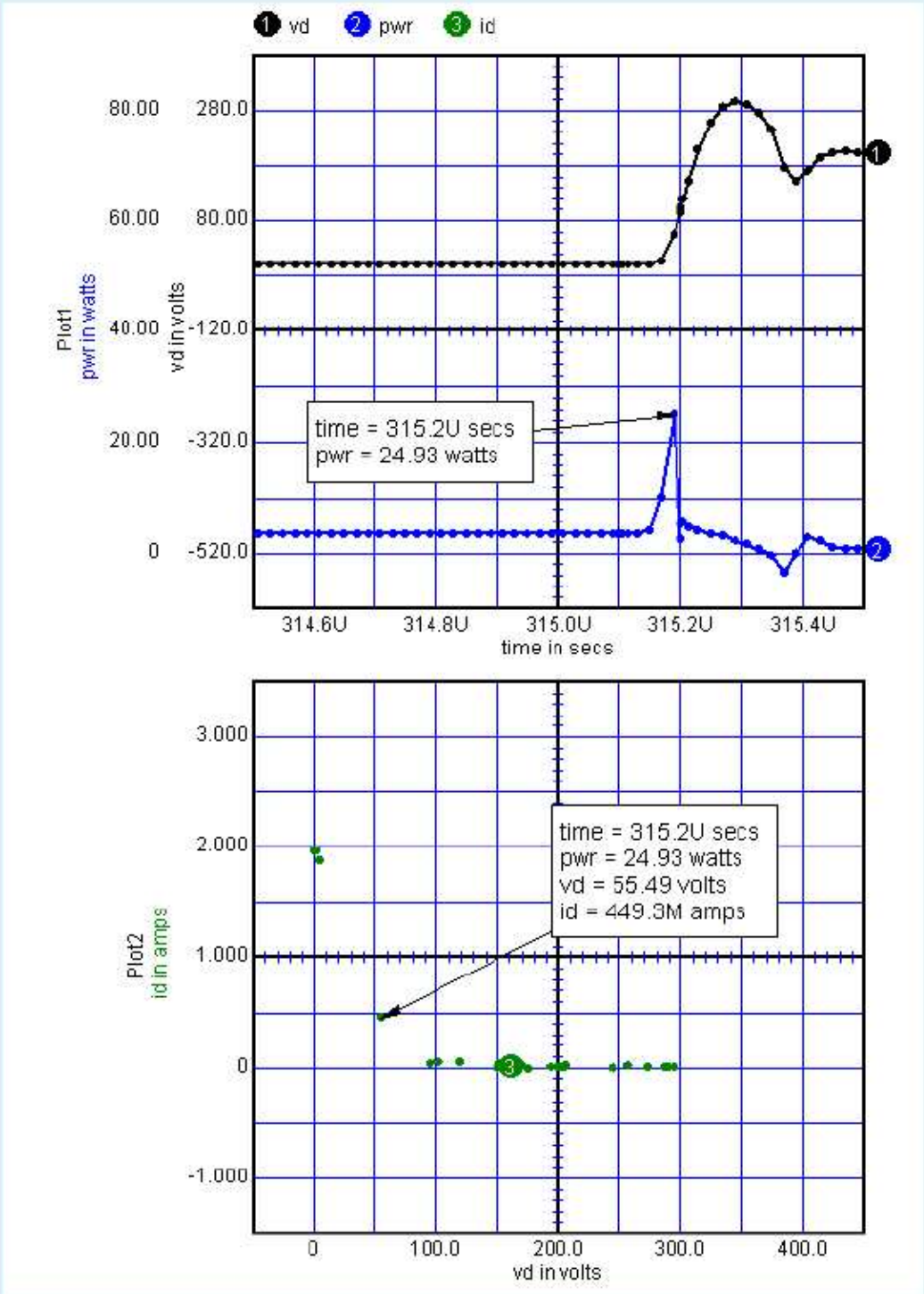

Figure 7. This power supply model uses standard OPTIONS versus VSECTOL for time step control.

Result using standard OPTIONS to control the time step produces lower accuracy during the turn-off transition and uses excessive computational resources when there is no switching activity.

<Using VSECTOL>

Circuits that switch states behaviorally won't interact with the IsSpice time step control algorithms. VSECTOL solves this problem by reducing the time step to maintain volt-second accuracy. This algorithm allows a much large MAXSTEP setting in the .TRAN control statement.

Originally, VSECTOL only checked the main circuit nodes. We subsequently included subcircuit nodes to the test. The way it works is for the simulator to take the absolute value difference of the predicted node voltage and the calculated node voltage and multiply the result by the time step. When the product is greater than the VSECTOL option, the time step is decreased. Hysteresis is used in the algorithm, to keep the time step from jumping back and forth. Here are some things to do when using VSECTOL to control the time step:

Set RELTOL=0.1 or greater
Disable BYPASS, see simulator options… more …Model
Normalize low voltage switching
Add switched current

Low voltage models for oscillators, logic gates and comparators are frequently used in the underlying macro models. To give these models the same weight as the higher voltage main circuit switches, its necessary to create dummy nodes that transform the voltage to a comparable value. Here's an example of a behavioral inverter

```
SUBCKT INV 1 2
B1 4 0 V= V(1)>3.5 ? 0 : 10V
RD 4 2 100
CD 2 0 10P
bvsectol 100 0 v=50*v(4)
rbvsectol 100 0 1k
.ENDS
```

bvsectol and rbvsectol were added to increase the VSECTOL sensitivity. Figure 9 shows the time step varying over one cycle of a Flyback Regulator simulation. The clock, shown in waveform 1 steps its transition down to under 15nSec rise and fall times and expands to about 1.5uSec when there is no switching activity. Notice the finer switching resolution near the Flyback interval near the center of the screen

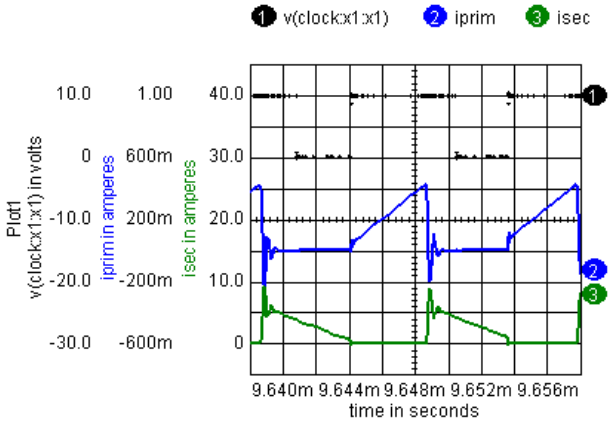

Figure 9. Variable time step control places computational power where it's needed.

Similarly, you can add B elements to make voltage nodes out of branch currents so that critical currents can also take advantage of the VSECTOL option. The diode current of D1 can be used as follows:

BD1 100 0 v=1k*I(D1)
RBD1 100 0 1k

IsSpice diodes can be made to switch on at nearly zero forward voltage by reducing their emission coefficient; for example, N=1m. Figure 10's I-V plot shows the difference between the default diode (waveform 2, N=1) and a low emission coefficient diode(waveform 1, N=1m).

Unfortunately, the diode equation is temperature dependant and low emission coefficients create numerical overflows when circuit temperature is changed even slightly. In IsSpice, the global circuit temperature of a diode can be overridden using the Temp=27 instance parameter. So when you use diodes with low emission coefficients, set Temp=27 in the diodes instance parameters and you will be able to vary circuit temperature and have your diode act as a nearly ideal switch.

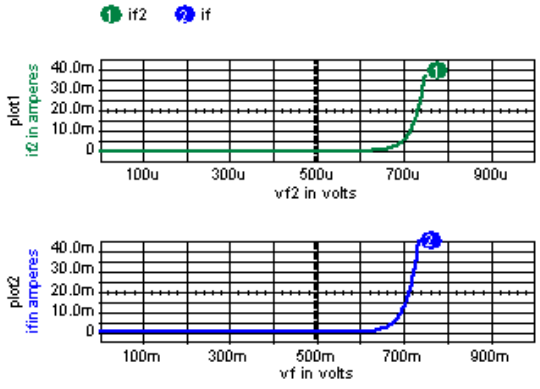

Figure 10. Low emission coefficient diodes are nearly ideal, conducting current at lower voltage.