

Bluetooth Module

HBM1X1M

Data Book

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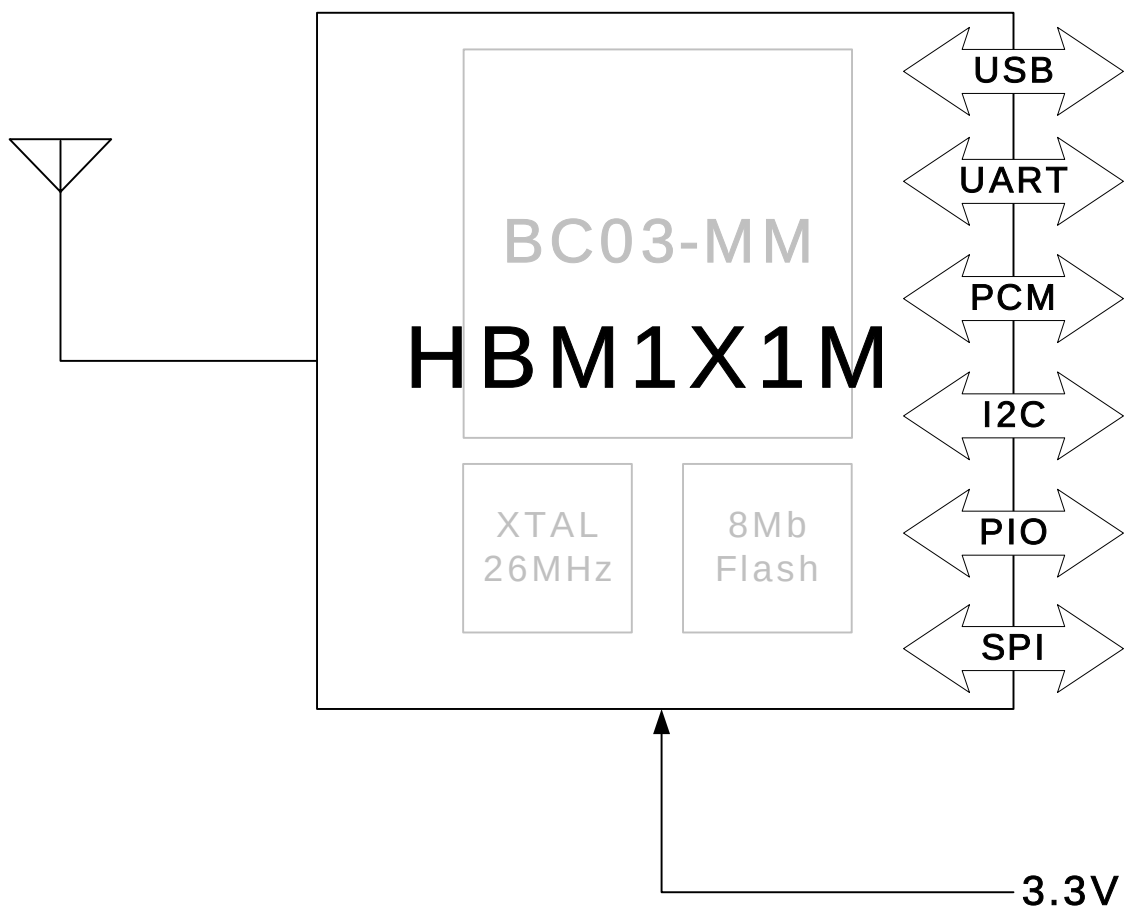
4 Application Schematic

1. General

1.1 Overview

This specification covers Bluetooth module (class-1) which complies with Bluetooth specification version 2.0 and integrates RF & Baseband controller in small package. This Module has deployed CSR's BC03-Multimedia External chipset.

All detailed specification including pinouts and electrical specification may be changed without notice.



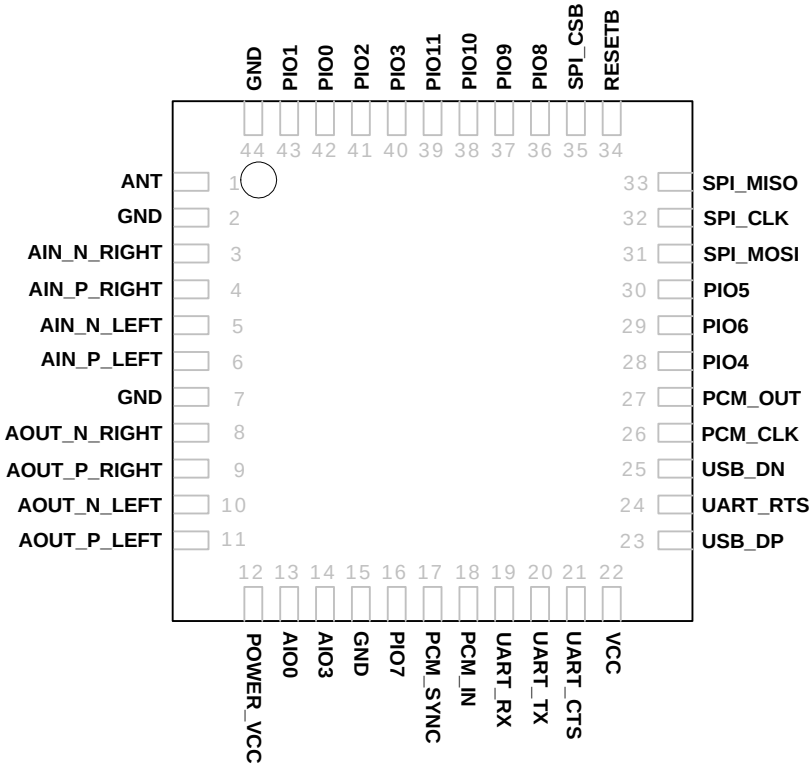
1.2 Features

- Fully Qualified Bluetooth System
- Bluetooth 2.0 Specification Compliant
- Kalimba DSP Open Platform Co-Processor
- Full Speed Bluetooth Operation with Full Piconet Support
- Operating Voltage 2.8~3.4V
- UART Interface With programmable baud rate up to 1.5Mbaud with an optional bypass mode
- Full Speed USB v1.1 Interface Supports OHCI And UHCI Host Interfaces
- 16-bit Resolution Stereo Audio Codec, Standard Sample Rates of 8kHz, 11.025kHz, 16kHz, 2.05kHz, 32kHz, 44.1kHz And 48kHz (DAC Only)
- Integrated Amplifiers For Driving Microphone And Speakers With Minimum External Components
- Standard HCI (UART and USB) support
- Fully Embedded RFCOMM
- External 8Mbit Flash Memory
- Integrated 26MHz Reference Clock
- Competitive Size (11.6mm x 11.6mm x 1.6mmT : LGA 44Pin)

1.3 Application

- Automotive Hands-Free Kits
- Echo Cancellation
- High Performance Telephony Headsets
- A/V Profile Support
- Access Point

1.4 Pin Configuration & Outline



HBM1X1M Pin Configuration



HBM1X1M Outline

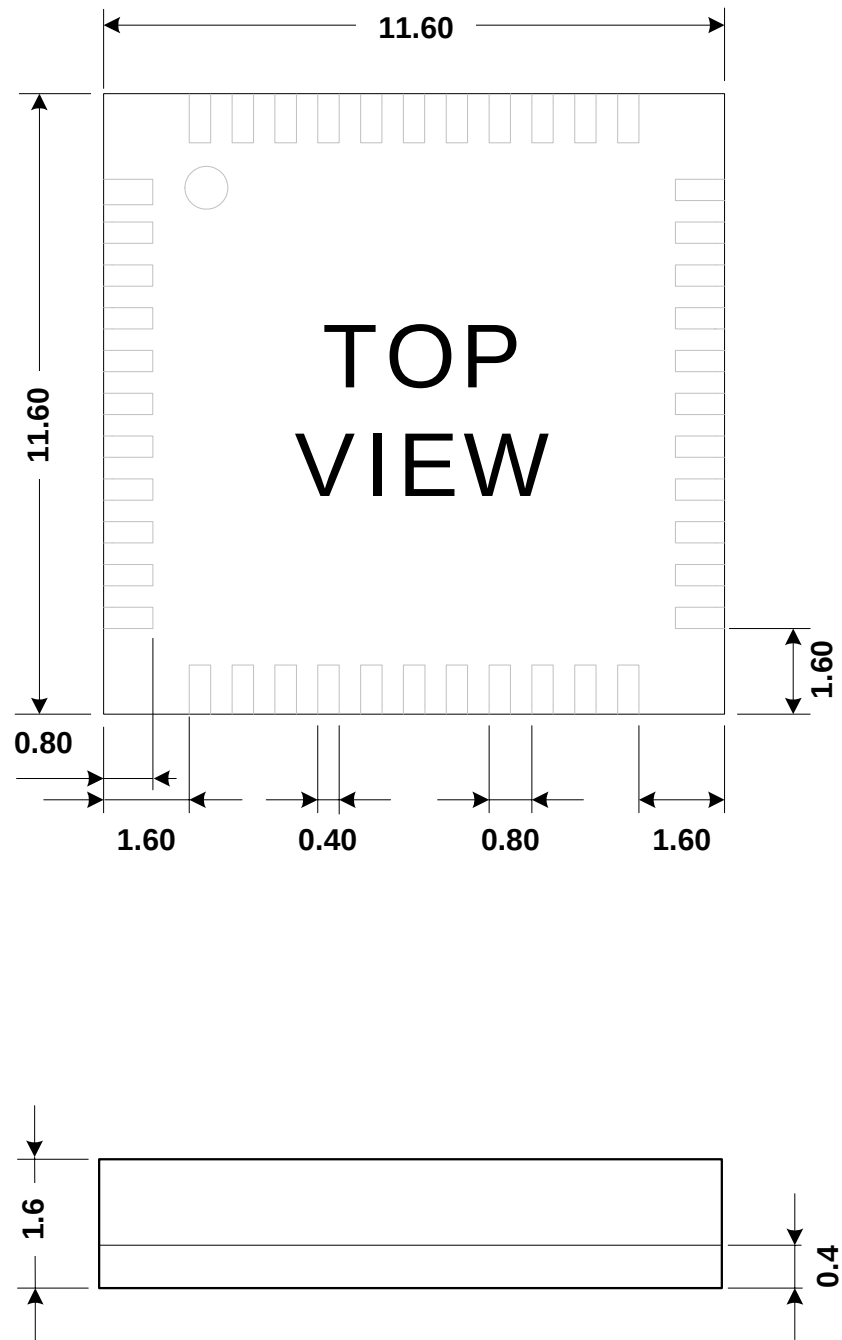
1.5 Device Terminal Functions

Function	Pin Name	PIN No	Description
PCM Interface	PCM_OUT	27 / G13	Synchronous data output
	PCM_IN	18 / J11	Synchronous data input
	PCM_CLK	26 / H13	Synchronous data clock
	PCM_SYNC	17 / H11	Synchronous data sync
UART Interface	UART_TX	20 / J12	UART data output
	UART_RX	19 / K11	UART data input (idle status high)
	UART_RTS	24 / L12	UART request to send, active low
	UART_CTS	21 / K12	UART clear to send, active low
SPI Interface	SPI_CSB	35 / C11	Chip select for Synchronous Serial Interface Active low
	SPI_CLK	32 / C13	Serial Peripheral Interface clock
	SPI_MISO	33 / B13	Serial Peripheral Interface data output
	SPI_MOSI	31 / D12	Serial Peripheral Interface data input
USB Interface	USB_DN	25 / K13	USB data minus
	USB_DP	23 / L13	USB plus with selectable internal 1.5K pull-up resistor
PIO Interface	PIO0	42 / C1	Don't use this pin, this pin is used for controlling external PA & LNA
	PIO1	43 / B1	Don't use this pin, this pin is used for controlling external PA & LNA
	PIO2	41 / C2	Programmable input/output line
	PIO3	40 / B2	Programmable input/output line
	PIO4	28 / F12	UART Bypass(UART_TX)
	PIO5	30 / F11	UART Bypass(UART_RTS)
	PIO6	29 / F13	UART Bypass(UART_CTS) / E2PROM(SCL)
	PIO7	16 / G11	UART Bypass(UART_RX) / E2PROM(SDA)
	PIO8	36 / D3	E2PROM (write protect)
	PIO9	37 / C3	Programmable input/output line
	PIO10	38 / B3	Programmable input/output line
	PIO11	39 / A3	Programmable input/output line

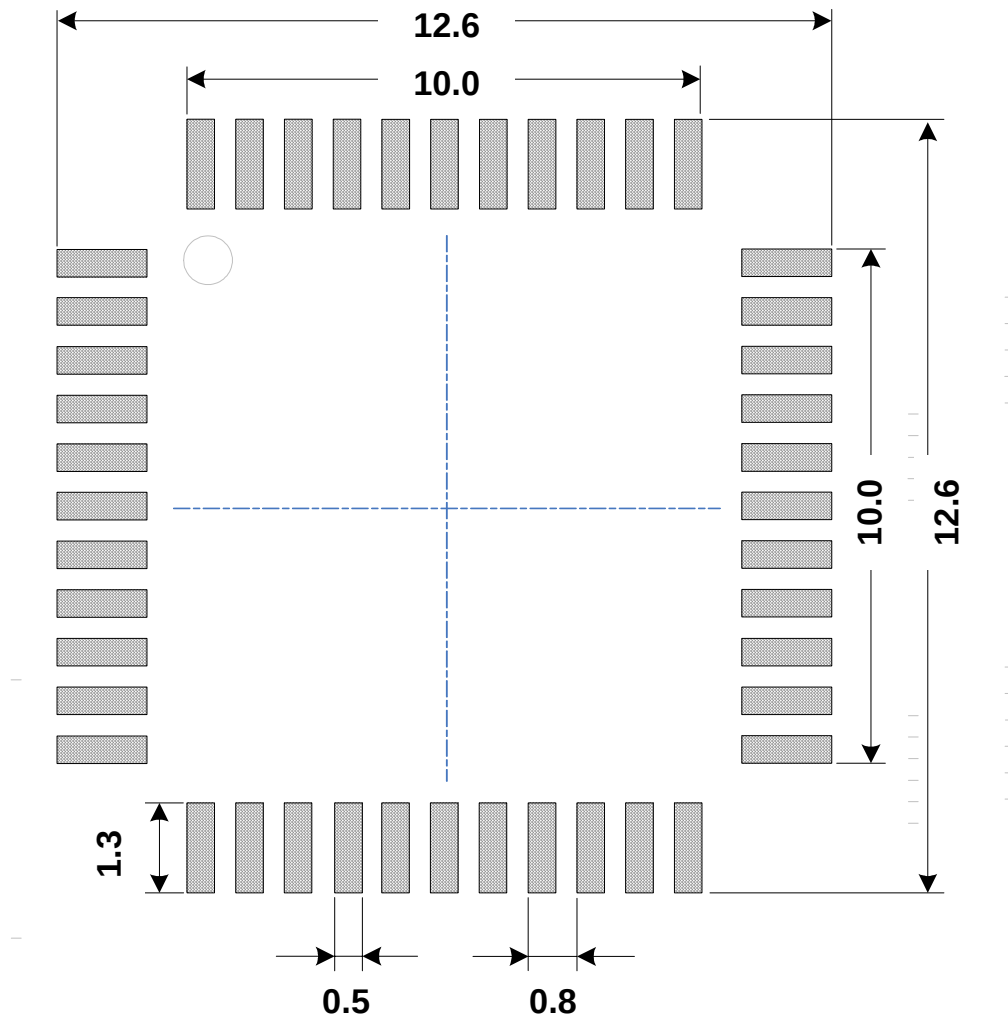
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AUDIO Interface	AIN_N_RIGHT	3 / M3	Microphone input negative(right side)
	AIN_P_RIGHT	4 / L3	Microphone input positive(right side)
	AIN_N_LEFT	5 / K3	Microphone input negative (left side)
	AIN_P_LEFT	6 / J3	Microphone input positive (left side)
	AOUT_N_RIGHT	8 / L2	Speaker output negative (right side)
	AOUT_P_RIGHT	9 / M2	Speaker output positive (right side)
	AOUT_N_LEFT	10 / L1	Speaker output negative (left side)
	AOUT_P_LEFT	11 / M1	Speaker output positive (left side)
Others	AIO0	13 / N3	General purpose analogue interface
	AIO3	14 / N4	General purpose analogue interface
	RESETB	34 /E12	Reset if low. Input debounced so must be low For > 5ms to cause a reset
	ANT	1 / E1,F1,G1	RF Connection to Antenna
	VCC	22	D.C Input voltage for operation (2.8~3.4V)
	POWER_VCC	12	D.C Input voltage for operation (2.8~3,4V)
	GND	2,7,15,44	Ground

1.6 Package Dimensions



1.7 Land Pattern Recommendation



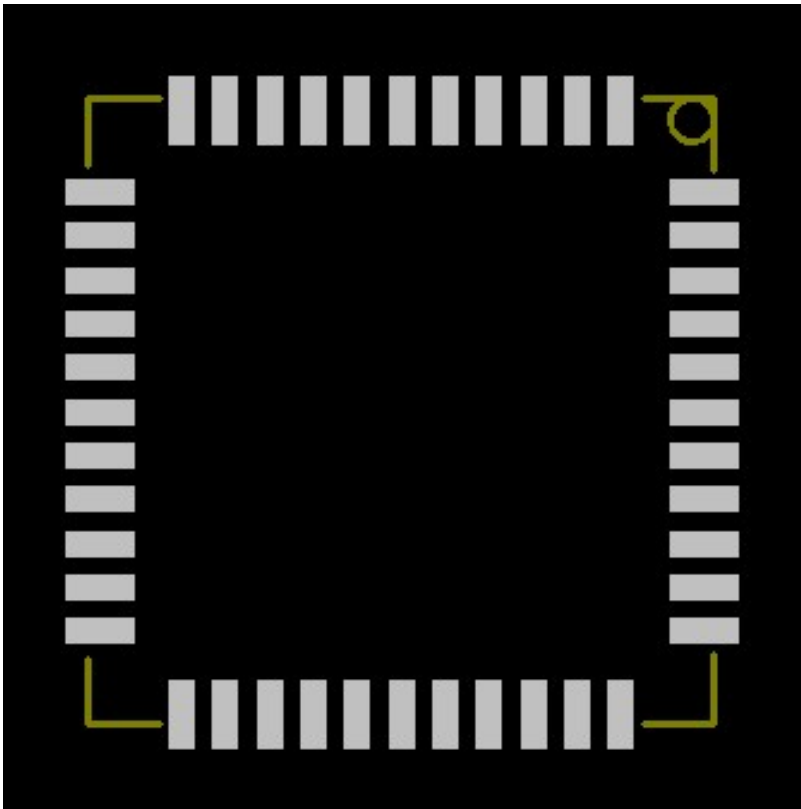
LAND PATTERN RECOMMENDATION

1.8 Recommended Metal Mask Condition

Optimized Bottom Solder Pad Size & Pin Pad Size

1.8.1 Pin Pad Size vs Metal Mask Opening Size : 1 vs 0.8

1.8.2 Metal Mask Thickness : 0.1mm



2 Characteristics

2.1 Electrical Characteristics

Absolute Maximum Ratings		
Rating	Minimum	Maximum
Storage temperature	-40℃	85℃
Supply voltage : VCC	-0.4V	3.6V
Other terminal voltages	VSS-0.4	VCC+0.4V

Recommended Operating Conditions		
Operating Conditions	Minimum	Maximum
Operating temperature range	-30℃	80℃
Supply voltage range		
VCC	2.8V	3.4V
POWER_VCC	2.8V	3.4V

2.2 Power Consumption

Operation Mode	Connection Type	UART Rate (Kbits/s)	Average	Unit
Inquiring mode	--	115.2	64	mA
ACL data transfer no traffic	Master	115.2	13	mA
ACL data transfer with file transfer	Master	115.2	46	mA
SCO connection HV3	Master	115.2	50	mA
SCO connection HV3	Slave	--	75	mA
ACL connection	Slave	--	75	mA
Standby Host connection	--	115.2	0.02	mA

Note :

Conditions : 25℃, 3.3V supply

2.3 RF Characteristics

Transmitter

Specification	Condition	Min	Typ	Max	Unit
Output power	Normal	16	17	20	dBm
Power density	Normal	14	15	18	dBm
Power control	Normal	2	4	8	dBm
Frequency range	Normal	2400	-	2483.5	MHz
20dB bandwidth for modulated carrier	Normal	-	950	1000	KHz
Adjacent channel power	±2MHz	-	-	-20	dBm
	±3MHz	-	-	-40	
Modulation Characteristics	Δf_{1avg}	140	165	175	KHz
	Δf_{2max}	115	150		KHz
	$\Delta f_{2avg} / \Delta f_{1avg}$	80			%
Initial carrier frequency tolerance	Normal	-20	-	20	KHz
Carrier frequency Drift	One slot packet(DH1)	-25	-	25	kHz
	Five slot packet(DH5)	-40	-	40	

Transceiver

Specification	Condition	Min	Typ	Max	Unit
Out of band spurious emissions	30MHz ~ 1GHz			-36	dBm
	1GHz ~12.75GHz			-30	
	1.8GHz ~5.1GHz			-47	
	5.1GHz ~5.3GHz			-47	

Receiver

Specification	Condition	Min	Typ	Max	Unit
Sensitivity level (0.1% BER)	Single slot packets	--	-87	-89	dBm
Sensitivity level (0.1% BER)	Multi slot packet	--	-87	-89	dBm
C/I performance	co - channel	-	-	11	dB
	1MHz (Adjacent channel)	-	-	0	
	2MHz (2 nd Adjacent channel)	-	-	-30	
	≥3MHz (3 rd Adjacent channel)	-	-	-40	
Blocking performance	30MHz ~ 2000MHz	-10	-	-	dBm
	2000MHz ~ 2400MHz	-27	-	-	
	2500MHz ~ 3000MHz	-27	-	-	
	3000MHz ~ 12.75GHz	-10	-	-	
Intermodulation performance	n = 5	-39		-	dBm
Maximum input level		-20	-10	-	dBm

3 Terminal Descriptions

3.1 UART

Four signals are used to implement the UART function. UART_TXD and UART_RXD transfer data between the two devices. The remaining two signals, UART_CTS and UART_RTS, can be used to implement RS232 hardware flow control where both are active low indicators.

3.1.1 UART Setting

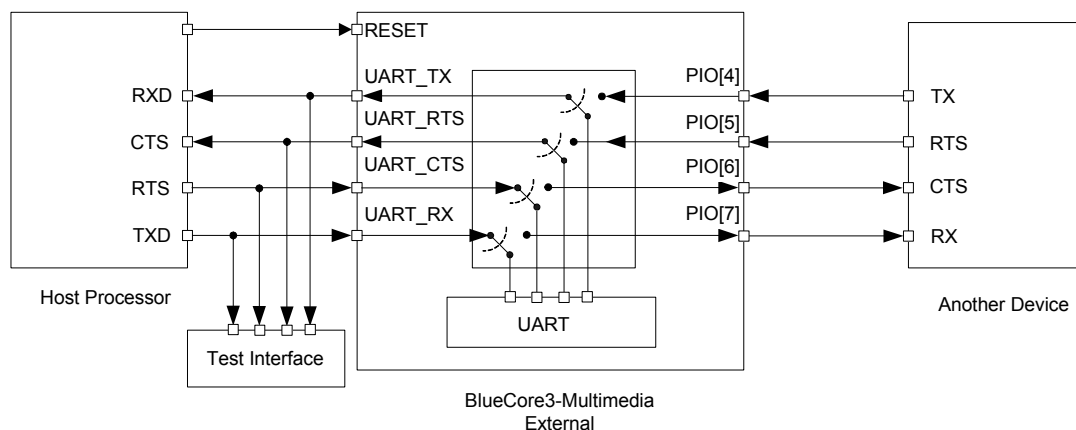
User can change data format the following selection using PSKEY. However, host shall communicate with default setting UART connection initiated at first time.

$$\text{Baud Rate} = (\text{PSKEY_UART_BAUD_RATE}) / 0.004096$$

Parameter	Possible value
Baud Rate	9600 ~ 1.5M Baud
Flow Control	RTS/CTS or None
Parity	None, Odd or Even
Number of Stop Bits	1 or 2
Bits per channel	8

3.1.2 UART Bypass Mode

Switch the bypass to PIO[7:4] as shown in figure. When the bypass mode has been invoked, module enters the deep sleep state indefinitely.



3.2 USB

This Bluetooth module contains a full speed (12Mbit/s) USB interface that is capable of driving a USB cable directly. No external USB transceiver is required. The device operates as a USB peripheral, responding to requests from a master host controller such as a PC. Both the OHCI and the UHCI standards are supported. The set of USB endpoints implemented can behave as specified in the USB section of the Bluetooth specification v1.2 or alternatively can appear as a set of endpoints appropriate to USB audio devices such as a set of USB speakers.

Since USB is a master/slave oriented system (in common with other USB peripherals), This Module only supports USB slave operation.

3.3 SPI (Serial Peripheral Interface)

BlueCore3-Multimedia External uses 16-bit data and 16-bit address serial peripheral interface, where transactions may occur when the internal processor is running or is stopped.

The BlueCore3-Multimedia External is the slave and receives commands on SPI_MOSI and outputs data on SPI_MISO.

1	Reset the SPI interface	Hold SPI_CSB high for two SPI_CLK cycles
2	Write the command word	Take SPI_CSB low and clock in the 8 bit command
3	Write the address	Clock in the 16-bit address word
4	Write or read data words	Clock in or out 16-bit data word(s)
5	Termination	Take SPI_CSB high

3.4 Kalimba DSP

The Kalimba DSP is an open platform Kalimba DSP allowing signal processing functions to be performed on over-air data or CODEC data in order to enhance audio applications.

The key features of the DSP include:

- 32MIPS performance, 24-bit fixed point DSP Core
- Single cycle MAC of 24 x 24-bit multiply and 56-bit accumulate
- 32-bit instruction word
- Separate program memory and dual data memory, allowing an ALU operation and up to two memory accesses in a single cycle
- Zero overhead looping and branching
- Zero overhead circular buffer indexing
- Single cycle barrel shifter with up to 56-bit input and 24-bit output
- Multiple cycle divide (performed in the background)
- Bit reversed addressing
- Orthogonal instruction set
- Low overhead interrupt

3.5 Audio Interface

The audio interface circuit consists of a stereo audio CODEC, dual audio inputs and outputs, and a PCM, I²S or SPDIF configurable interface.

The interface for the digital audio bus shares the same pins as the PCM CODEC Interface :

PCM Interface	SPDIF Interface	I ² S Interface
PCM_OUT	SPDIF_OUT	SD_OUT
PCM_IN	SPDIF_IN	SD_IN
PCM_SYNC		WS
PCM_CLK		SCK

3.6 Stereo Audio Interface

The main features of the interface are:

- Stereo and mono analogue input for voice band and audio band
- Stereo and mono analogue output for voice band and audio band
- Support for stereo digital audio bus standards such as I2S
- Support for IEC-60958 standard stereo digital audio bus standards i.e.

S/PDIF and AES3/EBU

- **Support for PCM interfaces including PCM master CODECs that require an external system clock**

3.7 PCM CODEC Interface

Pulse Code Modulation (PCM) is a standard method used to digitize audio (particularly voice) patterns for transmission over digital communication channels. Through its PCM interface, this module has hardware support for continual transmission and reception of PCM data, so reducing processor overhead for wireless headset applications. This module offers a bi-directional digital audio interface that route directly into the baseband layer of the on-chip firmware. It dose not pass through the HCI protocol layer.

Hardware allows the data to be sent to and received from a SCO connection

This module interfaces directly to PCM audio devices including the following :

- **Qualcomm MSM 3000 series and MSM 5000 series CDMA baseband devices**
- **OKI MSM7705 for channel A-law and u-law CODEC**
- **Motorola MC145481 8-bit A-law and u-law CODEC**
- **Motorola MC145483 13-bit linear CODEC**
- **STW 5093 and 5094 14-bit linear CODECs**

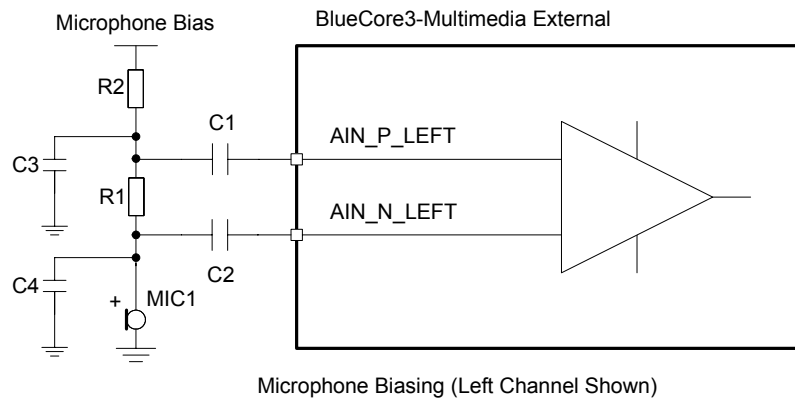
3.7.1 PCM Configuration

The PCM configuration is set using two PS keys, PSKEY_PCM_CONFIG32 and PSKEY_PCM_LOW_JITTER_CONFIG. The default for long frame sync and interface master generating 256KHz PCM_CLK with no tristating of PCM_OUT.

Parameter	Possible value
Mode	Slave, Master
Clock Rate	Master Mode : 128, 256, 512KHz Slave Mode : up to 2048KHz
Sync Formats	Long frame sync, Short frame sync
Data Formats	13 or 16bit linear, 8 - bit A - law to u - law

3.8 Microphone Input

The audio-input is intended for use from $1\mu\text{A}@94\text{dB SPL}$ to about $10\mu\text{A}@94\text{dB SPL}$. With biasing-resistors R1 and R2 equal to $1\text{k}\Omega$, this requires microphones with sensitivity between about -40dBV and -60dBV .



5 Application Schematic

